AMENDMENTS TO THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

Listing of the Claims:

1. (Original) A mold die for molding a semiconductor device package comprising:

a cavity block, the cavity block including a concave surface defining a cavity in which a semiconductor chip may be positioned, the semiconductor chip being generally rectangular and having a top surface and bottom surface and four side surfaces;

a gate, the gate defining a mold resin entry into the cavity and having a gate width; and

a gate block arranged and configured for movement relative the cavity block to provide selective opening and closing of the gate,

wherein the gate is arranged relative to the semiconductor chip whereby mold resin entering the cavity through the gate will contact the side surfaces of the semiconductor chip at an angle of less than about 70°.

2. (Original) A mold die for molding a semiconductor device package according to claim 1, wherein:

the cavity defined in the cavity block is substantially rectangular and has side walls;

the semiconductor chip is oriented with the side surfaces generally parallel to closest side wall of the cavity.

3. (Original) A mold die for molding a semiconductor device package according to claim 1, wherein:

the cavity defined in the cavity block has four side wall segments and three corners defining a first portion of a cavity perimeter;

the semiconductor chip being oriented with the side surfaces generally parallel to the closest side wall segments; and

the gate block, when closed, forms a second portion of the cavity perimeter.

4. (Original) The mold die for molding a semiconductor device package according to claim 1, wherein:

the cavity perimeter is substantially rectangular when the gate block is closed.

5. (Original) The mold die for molding a semiconductor device package according to claim 3, wherein:

the gate block includes an internal surface that provides the second portion of the cavity perimeter, the internal surface being positioned between a first side wall segment and a second side wall segment defined by the cavity block, and

further wherein the internal surface includes an inclined portion that is not parallel to the first or the second side wall segments.

6. (Original) The mold die for molding a semiconductor device package according to claim 5, wherein:

the internal surface further includes a first portion that is substantially parallel to the first side wall segment and a second portion that is substantially parallel to the second side wall segment.

7. (Original) The mold die for molding a semiconductor device package according to claim 5, wherein:

the internal surface is substantially identical to the inclined portion of the internal surface, the gate width is substantially identical to a length of the inclined portion.

8. (Currently Amended) The mold die for molding a semiconductor device package according to claim 3, wherein:

a third side wall segment is positioned opposite and generally parallel to the first side wall segment, the third side wall segment being longer than the first side wall segment;

a fourth side wall segment is positioned opposite and generally parallel to the second side wall segment, the fourth side wall segment being longer than the second side wall segment; and

the gate width is at least equal to one-half of a first length ~~equal to the shorter of the third and fourth side wall segments~~ and is less than a second length, wherein the first length is equal to

the shorter of the third and fourth side wall segments and the second length is equal to the longer of the third and fourth side wall segments. ~~equal to the longer of the third and fourth side wall segments.~~

9. (Original) The mold die for molding a semiconductor device package according to claim 8, wherein:

the internal surface is symmetric about an axis extending from a corner of the cavity opposite the gate and extending through a center point of the cavity.

10. (Currently Amended) A mold die for molding a chip array package comprising:

a plurality of semiconductor chips;

a cavity block, the cavity block including a concave surface defining a cavity in which ~~a~~the plurality of semiconductor chips may be positioned, the plurality of semiconductor chips being generally rectangular and having a top surface and bottom surface and four side surfaces;

a gate, the gate defining a mold resin entry into the cavity and having a gate width; and

a gate block arranged and configured for movement relative the cavity block to provide selective opening and closing of the gate,

wherein the gate is arranged relative to the plurality of semiconductor chips whereby mold resin entering the cavity through the gate will contact the side surfaces of the plurality of semiconductor chips at an angle of less than about 70°.

11. (Original) A mold die for molding a chip array package according to claim 10, wherein:

at least two of the plurality of semiconductor chips are arranged in a stacked orientation with bonding wires providing electrical connection between an upper semiconductor chip and a lower semiconductor chip.

12. (Original) A molding apparatus for molding a chip array comprising:

a mold die according to claim 1 wherein the cavity is arranged and configured to receive a plurality of aligned semiconductor chips having side surfaces, and further wherein the gate is arranged and configured so that mold resin entering the cavity through the gate will approach the side surfaces ;

a pot for maintaining mold resin;

a channel block defining a fluid path between the pot and the gate block.

13. (Original) A molding apparatus for molding a plurality of chip arrays comprising:

a plurality of mold dies according to claim 1;

a pot for maintaining mold resin;

a channel block defining a plurality of fluid paths between the pot and the plurality of mold dies.

14. (Original) A method for molding a semiconductor device package using a mold die according to claim 1 comprising:

arranging a semiconductor chip within the cavity, the semiconductor chip having side surfaces;

moving the gate block to open a gate into the cavity;

injecting a flow of mold resin into the cavity through the gate to fill the cavity;

moving the gate block to close the gate;

solidifying the mold resin within the cavity to form the semiconductor device package; and

removing the semiconductor device package from the cavity,

wherein the gate is configured and positioned such that the flow of mold resin approaches the side surfaces at an angle of less than 90°.

15. (Original) A method for molding a semiconductor device package using a mold die according to claim 1 comprising:

arranging a semiconductor chip within the cavity, the semiconductor chip having side surfaces and a plurality of bonding wires arranged adjacent the side surfaces for providing electrical connection between the semiconductor chip and a substrate;

moving the gate block to open a gate into the cavity;

injecting a flow of mold resin into the cavity through the gate to fill the cavity;

moving the gate block to close the gate;

solidifying the mold resin within the cavity to form the semiconductor device package; and

removing the semiconductor device package from the cavity,

wherein the gate is configured and positioned such that the mold resin flows past all bonding wires adjacent a single side surface of the semiconductor chip in a generally uniform direction.

16. (Original) A method for molding a semiconductor device package using a mold die according to claim 15 comprising:

arranging a semiconductor chip within the cavity, the semiconductor chip having side surfaces and a plurality of bonding wires arranged adjacent the side surfaces for providing electrical connection between the semiconductor chip and a substrate, wherein the bonding wires are arranged so as to provide a region of low bonding wire density adjacent a first corner of the semiconductor chip;

wherein the gate is configured and positioned such that the mold resin separates into two flows as it reaches a second corner of the semiconductor chip, the second corner being located diagonally across the semiconductor chip from the first corner, the two mold resin flows recombining near the region of low bonding wire density.